ABSTRACT OF THE DISCLOSURE

A compiler apparatus is capable of generating instruction sequences causing a processor to operate with lower power consumption. The compiler apparatus translates a source program into a machine language program for a processor including execution units which can execute instructions in parallel, and including instruction issue units which issue the instructions executed, respectively, by the execution units. The compiler apparatus includes a parser unit operable to parse the source program, an intermediate code conversion unit operable to convert the parsed source program into intermediate codes, an optimization unit operable to optimize the intermediate codes to reduce a hamming distance between instructions from the same instruction issue unit in consecutive instruction cycles, and includes a code generation unit operable to convert the optimized intermediate codes into machine language instructions.